Novel adiabatic tapered couplers for active III-V/SOI devices fabricated through transfer printing

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Abstract: We present the design of two novel adiabatic tapered coupling structures that allow efficient and alignment tolerant mode conversion between a III-V membrane waveguide and a single-mode SOI waveguide in active heterogeneously integrated devices. Both proposed couplers employ a broad intermediate waveguide to facilitate highly alignment tolerant coupling. This robustness is needed to comply with the current misalignment tolerance requirements for high-throughput transfer printing. The proposed coupling structures are expected to pave the way for transfer-printing-based heterogeneous integration of active III-V devices such as semiconductor optical amplifiers (SOAs), photodetectors, electro-absorption modulators (EAMs) and single wavelength lasers on silicon photonic integrated circuits.

OCIS codes: (130.0250) Optoelectronics; (130.6622) Subsystem integration and techniques; (250.5300) Photonic Integrated Circuits.

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1. Introduction

In recent years silicon photonics has emerged as a mature platform for the integration of different optical functions. Thanks to its compatibility with complementary metal-oxide (CMOS) fabrication technology the platform has proven its usefulness for the realisation of small-footprint passive optical components such as high-confinement waveguides [1], grating couplers [2], Bragg gratings [3] and arrayed waveguide gratings (AWGs) [4] as well as active integrated components such as high-speed modulators [5] and photodetectors [6]. However, due to its indirect bandgap, silicon is in itself unsuitable for the realisation of optical sources. In the past decade there has therefore been considerable research in the area of heterogeneous III-V-on-silicon integration, whereby III-V semiconductor compounds are incorporated on the silicon-on-insulator (SOI) platform either through direct wafer bonding [7, 8] or adhesive DVS-BCB bonding techniques [9, 10]. These approaches are very suited for dense III-V integration on passive SOI waveguide circuits but are less efficient in terms of III-V material usage when a sparse integration of III-V is required. Furthermore, they are difficult to implement when III-V devices need to be integrated on full platform silicon photonic ICs comprising a thick back-end stack.

Micro-transfer-printing (μTP or just transfer printing) is a novel technique initially proposed by Rogers *et al.* [11] in 2004 that allows to transfer thin film components from a source to a target substrate. Shortly after its first introduction, several devices were successfully fabricated using the transfer printing technique. Examples include a quantum dots display on glass [12],

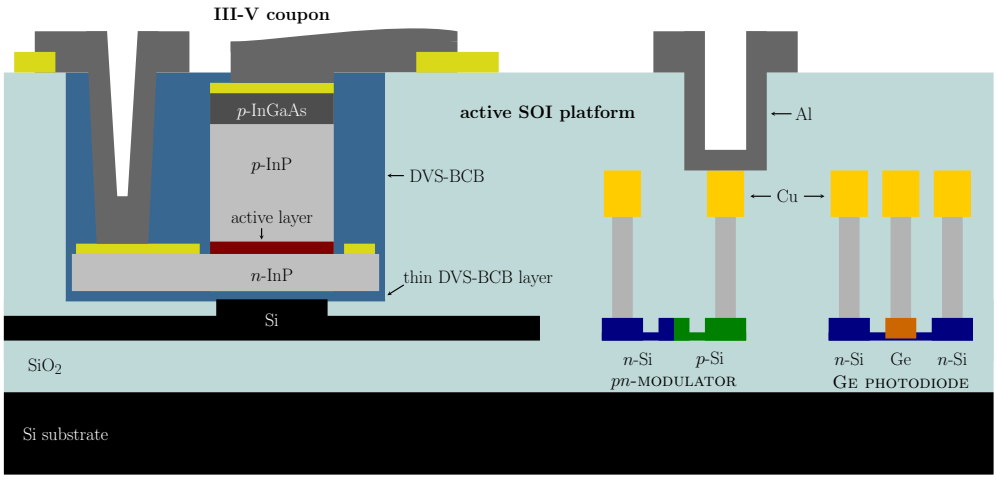

Figure 1. Overview of a typical active silicon photonic integration platform. A local opening in the back-end stack contains the processed III-V device coupon.

a stacked nano-membrane laser on silicon [13] and light-emitting diodes on diamond and glass substrates [14]. In the meanwhile, the technique has also been successfully employed to transfer processed III-V membranes such as Fabry-Pérot laser devices to a silicon substrate [15]. In transfer printing a soft elastomeric stamp is used to pick-and-place the desired device structures in a massively parallel fashion. Hence the technique serves as a promising alternative to the bonding approaches for III-V integration on full platform silicon photonic ICs. III-V devices can first be (partially) realised in dense arrays on their native substrate, after which they are released from the substrate and transferred in parallel to the silicon photonic target wafer. Through global wiring on the wafer scale the III-V/SOI device contacts are then connected to the metal contact pads. Figure 1 shows the layout of a typical active silicon photonic integration platform in which a local opening in the back-end stack is made for the processed III-V device coupon.

Figure 2 shows a schematic of the transfer printing process of a III-V patterned device onto a silicon target substrate. First the III-V device is patterned on its native substrate. This comprises typical III-V processing and includes the definition of the metal contacts. Afterwards polymer tethers are defined that anchor the device to the substrate. During subsequent underetching of the release layer the III-V device becomes free-standing, only anchored to the substrate at specific points. During device pickup the tethers then easily break at these anchor points. Finally the device is printed on the SOI target substrate. A thin DVS-BCB adhesive layer is used to planarize the SOI surface, which facilitates the printing process.

In order to efficiently couple light between the III-V waveguide layer and the silicon waveguide layer adiabatic tapered III-V/SOI couplers are commonly employed. Such optical coupling structures can be made highly efficient [16, 17, 18] and ultra-compact [19] but typically require a lateral alignment accuracy better than 300 nm [19, 20]. Currently the alignment accuracy in high-throughput transfer printing lies between 500 nm and 1 μm such that those conventional coupling structures are not suited for transfer printing. In this paper we propose two novel adiabatic tapered couplers that enable alignment-tolerant coupling for active III-V/SOI devices. In the manuscript we will provide an in-depth discussion of the coupler designs together with a detailed analysis of the different parameters that influence the coupling efficiency and alignment tolerance.

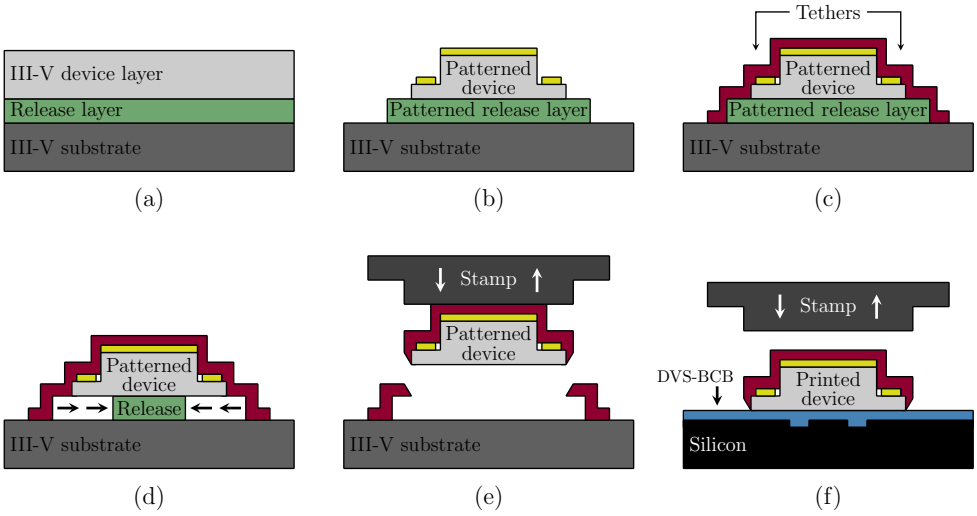

Figure 2. Process flow for transfer printing a III-V patterned device onto a silicon target substrate. (a) III-V source wafer; (b) Patterning of device and release layer; (c) Definition of tethers for device anchoring; (d) Removal of release layer; (e) Device pick-up from source; (f) Device release on target.

Table 1. Detailed III-V Epitaxial Layer Stack

Layer	Composition	Doping	Thickness (nm)	R.I. at 1550 nm
Cladding	InP	n.i.d.	1600	3.169
Passive quaternary	AlGaInAs	n.i.d.	300	3.325
Cladding	InP	n	$t_{n-\text{clad}}$	3.169

1.1. Technology platforms and simulation tools

In this paper *imec*'s active silicon photonic integration platform [21] is considered as the target wafer for the transfer printed devices. The SOI platform comes with a 160 nm thick polycrystalline silicon (p-Si) layer on top of a 220 nm thick monocrystalline silicon (c-Si) layer. Such a silicon waveguide layer thickness enables efficient light coupling from the III-V to the SOI waveguide in heterogeneously integrated III-V/SOI devices [16]. The silicon substrate and silicon device layer are separated by a 2 μm-thick buried oxide (BOX) layer.

For the III-V material an epitaxial stack is assumed that matches a typical 1550 nm optical amplifier epitaxial layer stack. The stack consists of an n-InP bottom cladding layer (thickness to be optimised, as discussed in the respective design sections), a 300 nm-thick AlGaInAs core layer and a 1.6 μm-thick InP top cladding. The stack is representative for a real active stack containing quantum wells and barriers but the AlGaInAs core and InP top cladding layers can also be considered to be passively regrown such that no electrical pumping of the coupler is required. In that case no p-doping of the InP top cladding is required. The details of the assumed epitaxial stack are shown in Table 1. Throughout this paper extensive use is made of the commercially available software FIMMWAVE, an optical mode solver from Photon Design. The EigenMode Expansion (EME) method is used to simulate the light propagation in the proposed coupling structures. All simulations are carried out for TE-polarized light at a wavelength of 1550 nm.

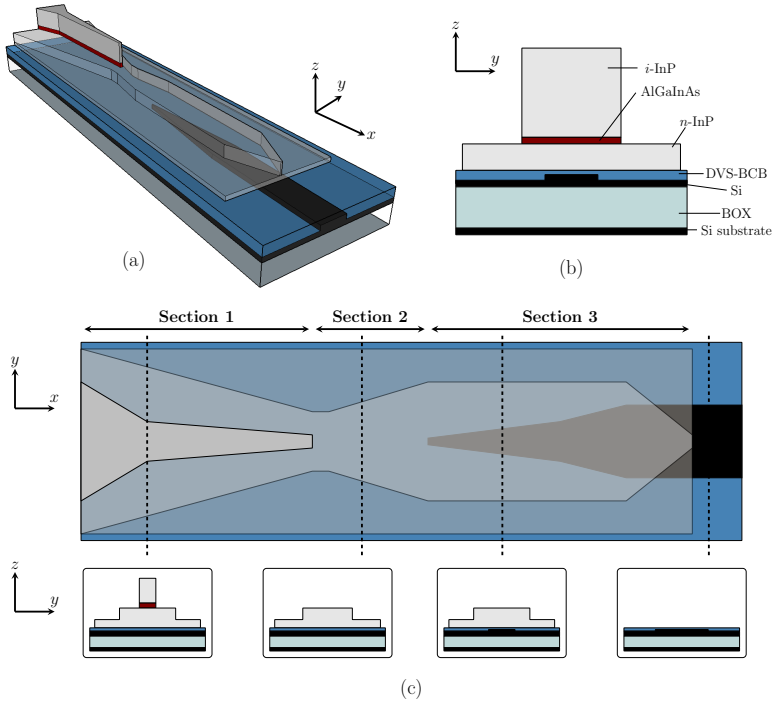

Figure 3. Schematic of the adiabatic tapered coupler. (a) 3D view; (b) Projected cross-sectional view with indication of the different layers; (c) Top view with cross-sectional views along the coupling structure.

1.2. Coupling mechanism

Just as in many commonly employed coupling structures, the mode conversion from the III-V waveguide to the SOI waveguide is based on adiabatic tapering [22]. By varying the waveguide dimensions along the structure, the effective indices of the fundamental local modes of the unperturbed waveguides (i.e. the III-V and SOI waveguide) can be increased or decreased. In this way the optical mode is gradually coupled from one waveguide to another. At the intermediate phase-matching point the energy of the optical mode is equally distributed over both waveguides. If the spatial waveguide variations occur gradual enough no light is coupled to higher-order modes and the tapering is said to be adiabatic.

2. Design of an adiabatic tapered coupler with broad *n*-InP intermediate waveguide

Figures 3(a)–3(c) show a detailed schematic of the first proposed adiabatic tapered coupler. The III-V waveguide structure is assumed to be transfer printed onto the SOI waveguide circuit using a DVS-BCB adhesive bonding layer. A passive regrown III-V stack is assumed in the taper such that no electrical pumping of the coupler is required. The structure comprises three tapered coupling sections that gradually transform the optical mode from the III-V waveguide to the silicon waveguide. The first coupling section consists of a two-step piecewise linear taper that converts the optical mode from the III-V waveguide to an InP rib waveguide implemented in the *n*-contact layer. The InP contact layer is *n*-doped and hence propagation losses due to free carrier absorption are small ($\alpha\ (1/\mathrm{cm}) \approx 10^{-18}\mathrm{cm}^2 N_D$, with N_D the doping ($1/\mathrm{cm}^3$) of the layer). The bottom slab of the *n*-InP rib waveguide is assumed to be 300 nm thick, which

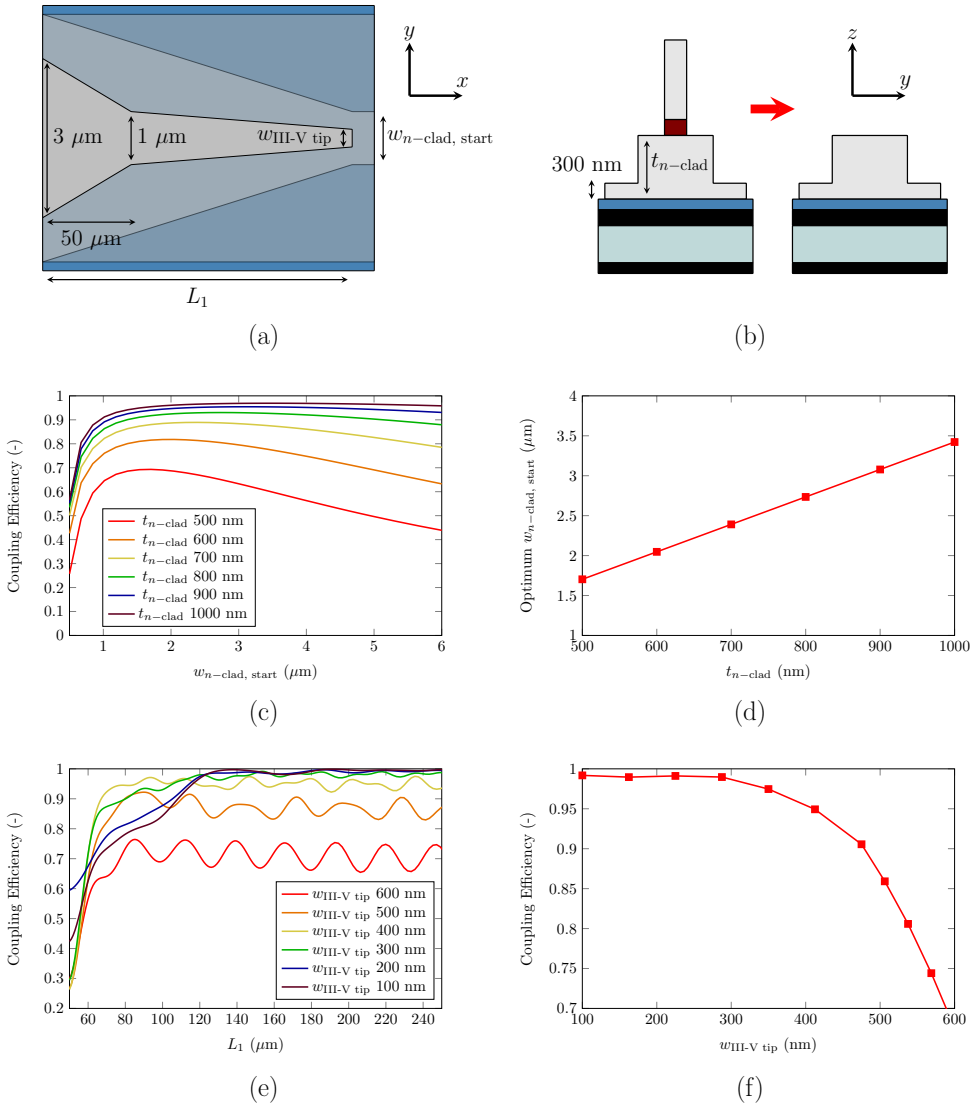

Figure 4. Optimisation of Coupling Section 1. (a) Schematic of Coupling Section 1; (b) Schematic of the interface at the end of Coupling Section 1; (c) Transmission at the interface at the end of Coupling Section 1 versus width of the *n*-InP rib waveguide for different thicknesses of the *n*-InP bottom cladding, $w_{\text{III-V tip}} = 400$ nm; (d) Optimum choice of the *n*-InP rib waveguide width versus thickness of the *n*-InP bottom cladding; (e) Taper coupling efficiency versus taper length for different values of the III-V taper tip width, $t_{n-\text{clad}} = 900$ nm and $w_{n-\text{clad, start}} = 3\ \mu$m; (f) Taper coupling efficiency versus III-V taper tip width for $L_1 = 150\ \mu$m, $t_{n-\text{clad}} = 900$ nm and $w_{n-\text{clad, start}} = 3\ \mu$m.

facilitates the transfer printing pick-up and release process. In the second coupling section a short linear taper increases the width of the *n*-InP waveguide to broaden the optical mode. This enhances the tolerance of the structure with respect to lateral misalignment of the III-V and the underlying silicon waveguide introduced by the transfer printing process. In the third coupling section another two-step piecewise linear taper (defined in silicon) is used to eventually couple the light to the silicon output waveguide. Finally the *n*-InP rib waveguide is tapered down to minimise reflections at the end of the coupling structure.

2.1. Optimisation of Coupling Section 1

The details of Coupling Section 1 are shown in Fig. 4(a). The optical mode initially resides in the III-V waveguide, which is assumed to be 3 μm wide. A two-step piecewise linear taper is used to gradually decrease the waveguide width such that the optical mode is adiabatically coupled to the $n-$InP rib waveguide. The intermediate waveguide width is chosen to be 1 μm. The length of the first taper part can be chosen as short as 50 μm. In the second part the actual coupling to the $n-$InP rib waveguide occurs, leading to a larger length of the second part of the taper. The coupling efficiency strongly depends on the dimensions of the *n*-InP rib waveguide and the achievable width of the III-V taper tip ($w_{\text{III-V tip}}$). Both dependencies are discussed below.

2.1.1. Choice of the *n*-InP cladding layer thickness

Figure 4(c) shows the coupling efficiency of the fundamental TE-mode of the III-V waveguide to the fundamental TE-mode of the butt-coupled *n*-InP rib waveguide versus width of the *n*-InP waveguide ($w_{n-\text{clad, start}}$), for different thicknesses of the *n*-InP cladding layer ($t_{n-\text{clad}}$). A schematic of the considered interface is shown in Fig. 4(b). A III-V taper tip width of 400 nm is assumed. As expected the transmission at the interface increases with increasing thickness of the *n*-InP cladding layer. Furthermore, for a given $n-$InP thickness an optimum width of the *n*-InP waveguide can be chosen for maximal transmission. This is because for a narrow (< 1 μm) *n*-InP waveguide the finite extent of the III-V taper tip prevents a high coupling efficiency whereas for very wide *n*-InP waveguides the mode mismatch at the interface increases, such that the coupling efficiency drops. Figure 4(d) shows the optimum *n*-InP waveguide width versus *n*-InP thickness. An *n*-InP thickness of 900 nm is chosen with a corresponding optimum *n*-InP waveguide width of 3 μm.

2.1.2. Influence of III-V taper tip width

The coupling efficiency is substantially influenced by the width of the III-V taper tip. Figure 4(e) shows the taper coupling efficiency versus taper length (L_1), for different III-V taper tip widths. The simulations are performed assuming the optimum dimensions obtained in section 2.1.1. The coupling efficiency saturates at a value determined by the butt-coupling of both waveguides. For taper tips narrower than 200 nm coupling is near to ideal. In practice III-V taper tip widths smaller than 400 nm are feasible to obtain with standard optical lithography and subsequent lateral underetching of the passive quaternary layer, as demonstrated in [23]. This yields a coupling efficiency of more than 96% for a taper length of 150 μm. Figure 4(f) shows the coupling efficiency versus III-V taper tip width for a fixed taper length of 150 μm. For taper tips wider than 500 nm the coupling efficiency already drops below 85%.

2.2. Optimisation of Coupling Section 2

The details of Coupling section 2 are shown in Fig. 5(a). The coupling section consists of a linear taper and serves to broaden the optical mode as to improve the alignment tolerance of the coupling structure. Based on the simulation results from section 2.1.1 the starting width of the

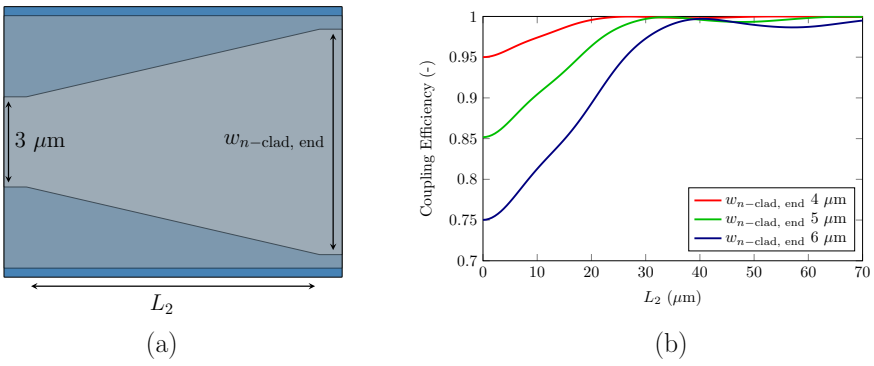

Figure 5. Optimisation of Coupling Section 2. (a) Schematic of Coupling Section 2; (b) Taper coupling efficiency versus taper length for different values of the InP waveguide end width.

n-InP waveguide is assumed to be 3 μm. The choice of the width of the *n*-InP end waveguide ($w_{n-\text{clad, end}}$) depends on the imposed alignment tolerance requirements. In general tapering to a wider *n*-InP rib waveguide will increase the alignment tolerance, at the expense of a slightly longer taper. In any case the length of Coupling Section 2 can be chosen very short, as is clear from Fig. 5(b). A taper length of 30 μm already suffices to achieve over 99% coupling efficiency for a width of the *n*-InP end waveguide of 4 μm. A 4 μm waveguide width is also assumed in the remainder of the manuscript. Note that the values for the coupling efficiencies at $L_2 = 0$ μm correspond with the coupling efficiencies for the 3 μm wide *n*-InP waveguide butt-coupled to the $w_{n-\text{clad, end}}$ wide *n*-InP waveguide.

2.3. Optimisation of Coupling Section 3

In Coupling Section 3 light is converted from the broad *n*-InP rib waveguide to the underlying silicon device layer. A schematic of Coupling Section 3 is shown in Fig. 6(a). A two-step piecewise linear silicon taper is used. At the end of the coupling structure the III-V waveguide is tapered down to enhance the coupling efficiency and to minimise reflections. This tapered section can be very short: a length of 30 μm suffices to achieve a good coupling efficiency. The coupling efficiency of Coupling Section 3 is greatly influenced by the III-V/silicon spacing (i.e. the thickness of the DVS-BCB adhesive layer) and the width of the silicon waveguide. The influence of both parameters is discussed below.

Figures 6(c) and 6(d) show the coupling efficiency of the fundamental TE-mode of the *n*-InP waveguide to the fundamental TE-mode of the silicon waveguide at the end of Coupling Section 3 versus silicon waveguide width, for different values of the III-V taper tip width and the DVS-BCB thickness. A schematic of the considered interface is shown in Fig. 6(b). As expected the coupling efficiency increases with increasing silicon waveguide width, as the mode becomes much stronger confined to the silicon waveguide. Figure 6(e) shows the coupling efficiency versus III-V taper tip width for different values of the DVS-BCB thickness. As the spacing between the III-V and silicon waveguide increases both waveguides are stronger decoupled and the coupling efficiency increases. Obviously a larger III-V/silicon spacing will also increase the taper length, which is not desired. The width of the silicon taper tip ($w_{\text{silicon tip}}$) is assumed to be 150 nm. This corresponds with the minimum reproducible dimension obtainable in a typical *imec* SOI run and only slightly influences the coupling efficiency. Simulations indicate that for silicon taper tip widths below 200 nm the coupling efficiency stays above 98%.

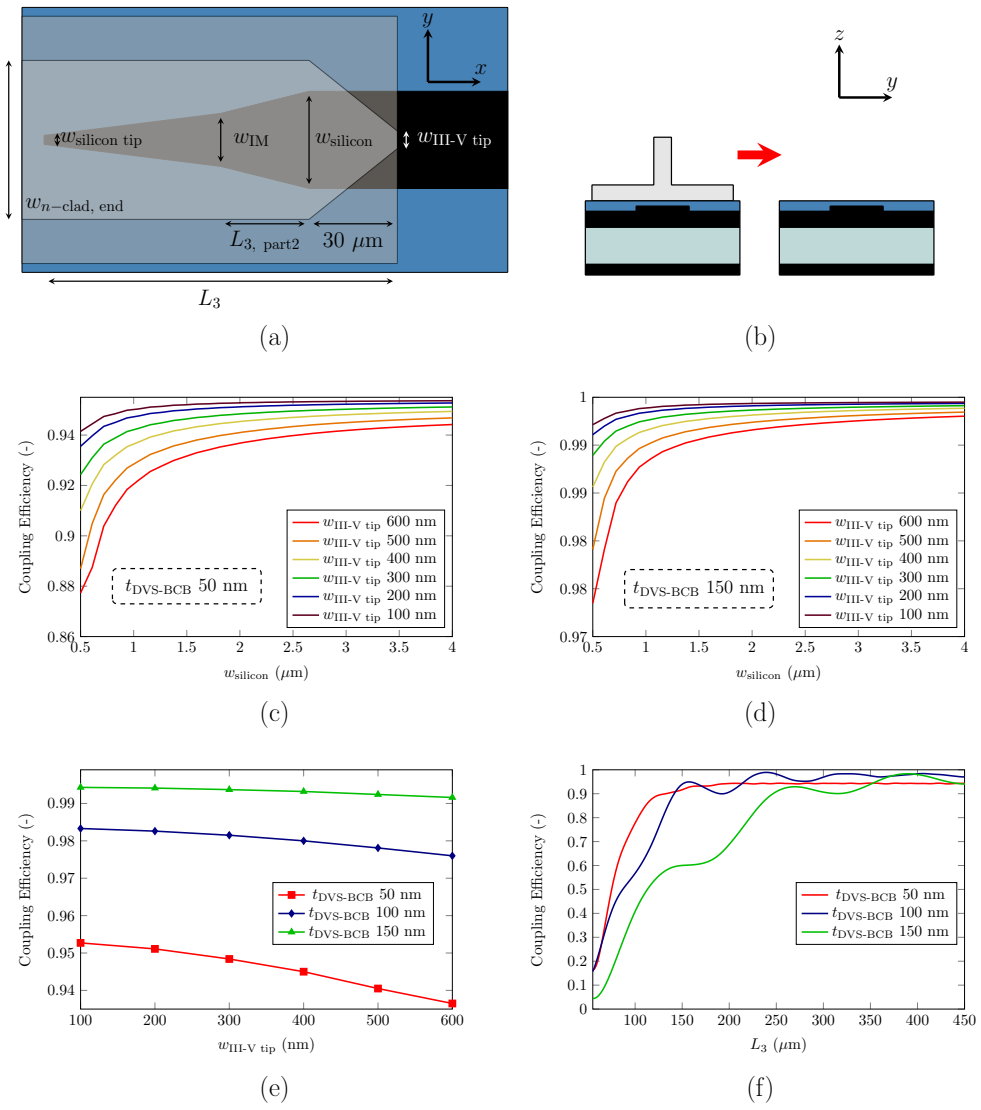

Figure 6. Optimisation of Coupling Section 3. (a) Schematic of Coupling Section 3; (b) Schematic of interface at the end of Coupling Section 3; (c) Transmission at the interface at the end of Coupling Section 3 versus width of the silicon waveguide for different values of the III-V taper tip width, $t_{\text{DVS-BCB}} = 50$ nm; (d) Transmission at the interface at the end of Coupling Section 3 versus width of the silicon waveguide for different values of the III-V taper tip width, $t_{\text{DVS-BCB}} = 150$ nm; (e) Transmission at the interface at the end of Coupling Section 3 versus III-V taper tip width for different values of the DVS-BCB thickness, $w_{\text{silicon}} = 2$ μm; (f) Taper coupling efficiency versus taper length for different values of the DVS-BCB thickness, $w_{\text{silicon}} = 2$ μm, $w_{\text{IM}} = 1.1$ μm.

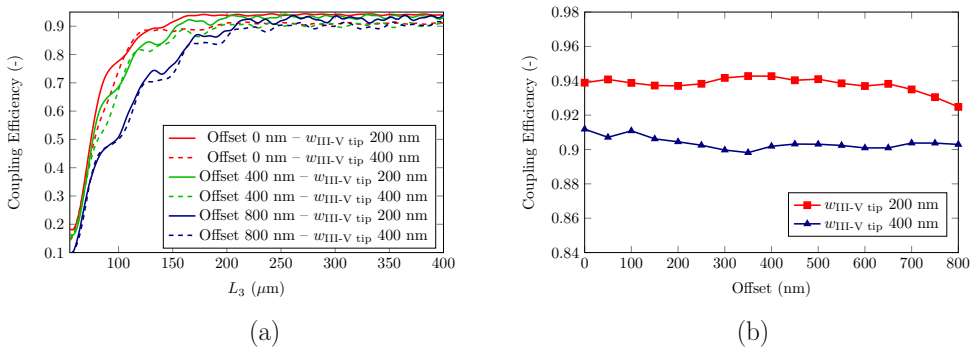

Figure 7. Overall coupling structure. (a) Coupling efficiency versus length of Coupling Section 3 (L_3) for different lateral alignment offsets and values of the III-V taper tip width; (b) Coupling efficiency versus lateral alignment offset for different values of the III-V taper tip width, $L_3 = 255$ μm.

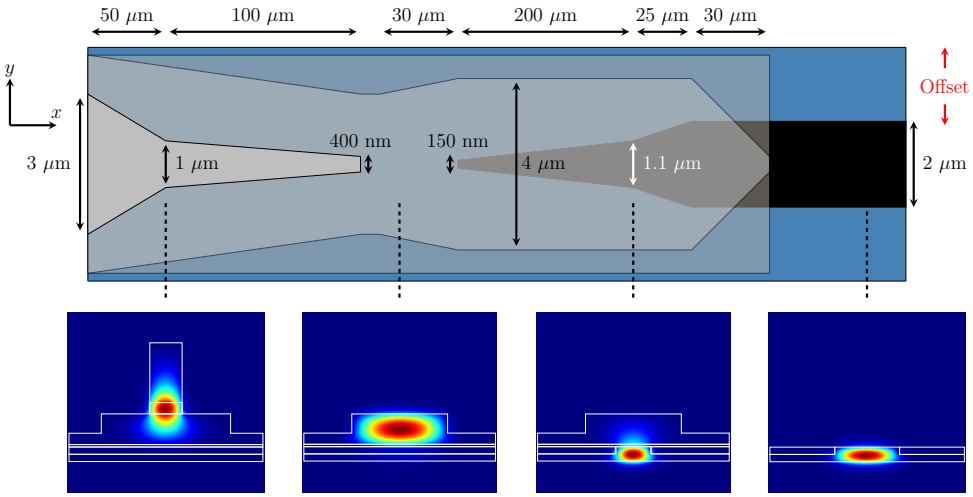

Figure 8. Overall coupling structure. Light propagation from the III-V waveguide to the SOI waveguide in the overall coupling structure for $w_{\text{III-V tip}} = 400$ nm. Mode profiles along the coupler are indicated as well.

Figure 6(f) shows the coupling efficiency versus taper length for different values of the DVS-BCB thickness. w_{IM} is chosen to be 1.1 μm, which is beyond the phase-matching point such that the mode is already well confined to the silicon waveguide at this point along the coupler. $L_{3,\text{ part 2}}$ can therefore be chosen as short as 25 μm. For modest DVS-BCB thicknesses (< 100 nm) and a silicon waveguide width of 2 μm a coupling efficiency of 94% is retrieved assuming a III-V taper tip width of 400 nm and a taper length (L_3) of 250 μm.

2.4. Overall coupling structure – lateral misalignment tolerance

Figure 7(a) shows the overall taper coupling efficiency versus taper length L_3 for different lateral alignment offsets (y-direction) of the silicon waveguide with respect to the III-V waveguide,

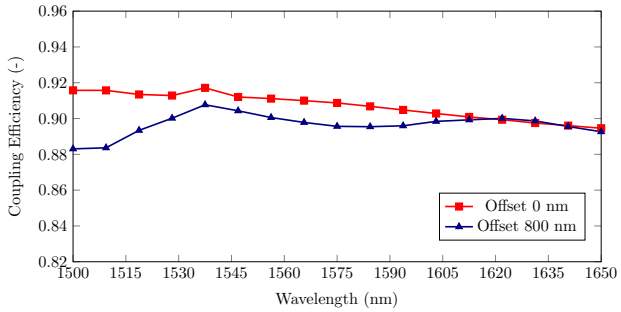

Figure 9. Wavelength dependence of the coupler efficiency for the overall optimised coupling structure with n-InP intermediate waveguide, $w_{\text{III-V tip}} = 400$ nm.

simulated for a III-V taper tip width of 200 nm and 400 nm. A DVS-BCB thickness of 50 nm is assumed. It is clear that for a given coupling efficiency a longer taper length is needed for a larger lateral alignment offset. However, at a taper length L_3 of 255 μm the coupling efficiency reaches values above 90%, even for a very large lateral alignment offset of 800 nm. This is a significant improvement as compared to previously reported coupling structures, which typically require a lateral alignment accuracy better than 300 nm. In Fig. 7(b) the coupling efficiency is shown versus lateral alignment offset for $L_3 = 255$ μm. A very robust performance is achieved with a coupling efficiency varying only a few percent with varying lateral alignment offset. Coupling to higher order modes remains below 1%, even for large lateral alignment offsets. Furthermore, by tapering down the silicon waveguide, the waveguide can be made single-mode such that guided higher-order modes will eventually radiate out and will not be present in the remaining optical circuit. Figure 8 shows the overall optimised coupling structure, assuming a III-V taper tip width of 400 nm. Mode profiles along the coupler show the adiabatic mode transformation from the III-V to the SOI waveguide. Finally Figure 9 shows the wavelength dependence of the coupler performance, both for a 0 nm and 800 nm lateral alignment offset. The simulations indicate that the coupling efficiency varies less than 5% over a broad wavelength range covering the C and L band. Finally the back reflections in the coupling structure are assessed. For taper tip widths between 200 nm and 400 nm and lateral alignment offsets between 0 nm and 800 nm the simulated back reflection remains smaller than -26 dB, which is adequate for most applications.

3. Design of an adiabatic tapered coupler with polymer intermediate waveguide

As an alternative we propose a coupling structure that does not require tapers to be etched in the III-V waveguide. Since no long coupling structures are present in the III-V, regrowth of a passive layer stack can be avoided. A schematic of the coupling structure is shown in Fig. 10(a). The III-V device is transfer printed onto the SOI chip using a 50 nm thick DVS-BCB adhesive bonding layer. To couple the light from the III-V waveguide into the silicon circuit layer, first, a butt-coupling approach is used to couple from the III-V waveguide into a polymer waveguide ($n = 1.69$). This polymer waveguide structure is post-processed after device transfer. The mode in the polymer waveguide structure is then coupled to the underlying 220 nm thick silicon slab waveguide using an inverted taper structure. A DVS-BCB ($n = 1.53$) overcladding of the whole structure is assumed.

By this coupling technique we avoid the transfer printing of fragile III-V tapers. Moreover, the length of the structures that need to be transfer printed is greatly reduced, resulting in more

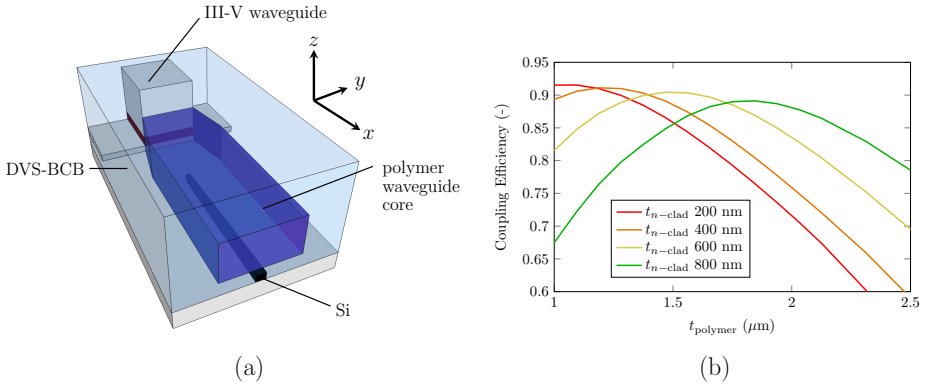

Figure 10. (a) Schematic of the adiabatic-taper-based coupling scheme using an intermediate polymer waveguide; (b) Butt-coupling efficiency at the III-V/polymer interface as a function of polymer waveguide thickness for different thicknesses of the *n*-InP bottom cladding. The III-V and polymer waveguide are assumed to be 5 μm wide.

robust fabrication.

The design of this coupling structure consist of two parts: the optimisation of the butt-coupling at the interface between the III-V waveguide and the polymer waveguide and the design of the adiabatic taper.

3.1. Optimisation of the butt-coupling efficiency at the III-V/polymer interface

In a first stage, the interface between the III-V waveguide and the polymer waveguide structure is assessed. To avoid unwanted Fresnel reflections at the III-V/polymer interface, the facet of the III-V waveguide is anti-reflection (AR) coated. A standard quarter wavelength AR coating is assumed. Figure 10(b) shows the coupling efficiency of the interface as a function of the polymer ($n = 1.69$) waveguide core thickness and the *n*-InP layer thickness. The III-V and polymer waveguide are assumed to be 5 μm wide. The optimal coupling efficiency is about 92% and is slowly decreasing with increasing *n*-InP thickness. The optimal polymer waveguide thickness increases with increasing *n*-InP thickness.

3.2. Optimisation of the SOI taper coupling section

The details of the SOI taper coupling section are shown in Figs. 11(a) and 11(b). The optical mode initially resides in the polymer waveguide, which is assumed to be 5 μm wide. While no tapering occurs in the polymer waveguide structure, the SOI waveguide structure tapers down to a narrow tip to achieve good coupling efficiency at the taper tip/polymer waveguide interface. The coupling efficiency strongly depends on the polymer thickness (t_{polymer}) and the width of the silicon taper tip ($w_{\text{silicon tip}}$).

In Figs. 11(c) and 11(d) the taper coupling efficiency is plotted as a function of the taper length for a taper tip width of 120 nm and 150 nm, respectively. In both cases, the thicker the polymer waveguide, the longer the taper should be before adiabatic taper coupling is achieved. Furthermore, an increase in taper tip width, results in an increase of the coupling efficiency for short tapers since the mode is pulled more strongly from the polymer to the silicon waveguide. However, a wider tip also results in higher losses at the coupling interface, thus the overall coupling efficiency for adiabatic coupling is lower for wider taper tips. This is also illustrated in Fig. 11(e). Moreover, increasing the polymer waveguide thickness slightly reduces the coupling

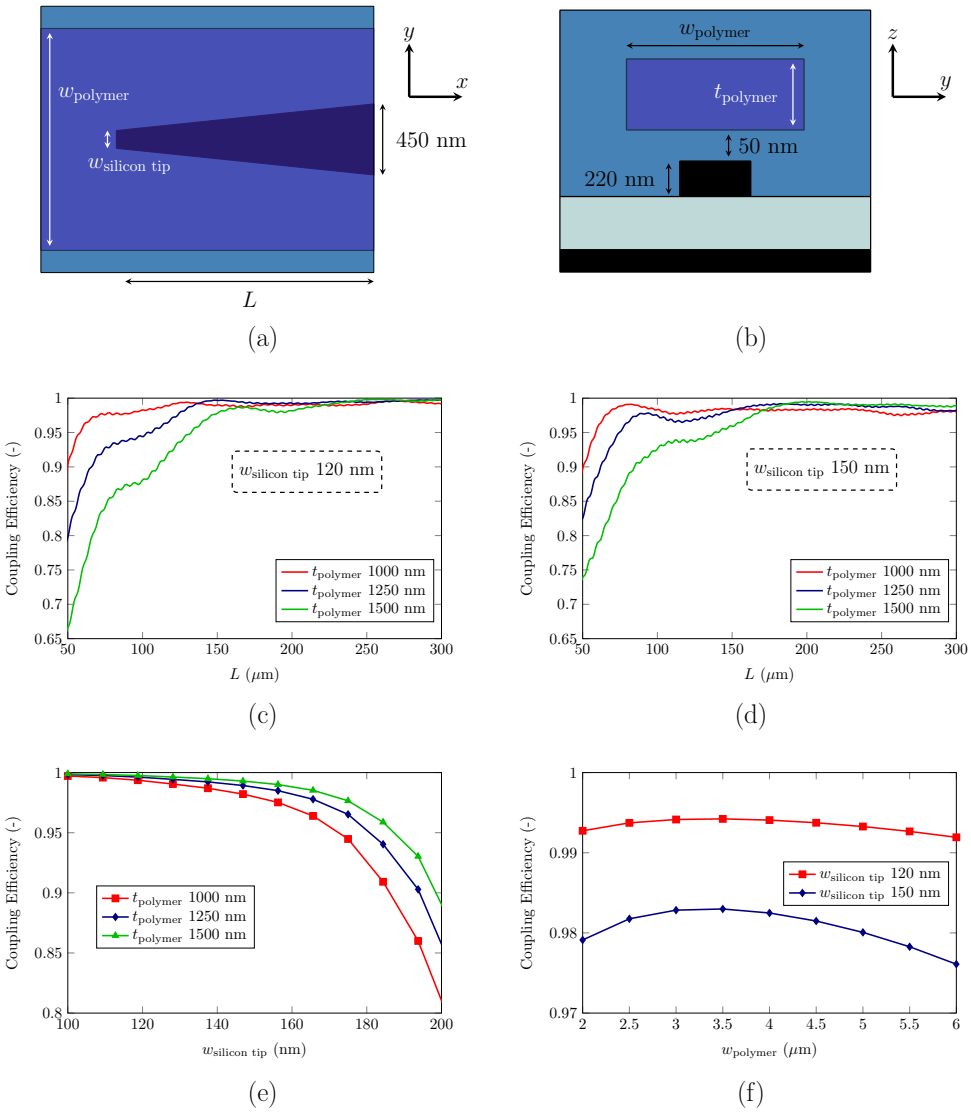

Figure 11. Optimisation of the SOI taper coupling section. (a) Top view of the taper coupling section; (b) Cross-sectional view along the taper; (c) Taper coupling efficiency versus taper length for different polymer thicknesses, $w_{\text{polymer}} = 5\ \mu$m and $w_{\text{silicon tip}} = 120$ nm; (d) Taper coupling efficiency versus taper length for different polymer thicknesses, $w_{\text{polymer}} = 5\ \mu$m and $w_{\text{silicon tip}} = 150$ nm; (e) Influence of the SOI taper tip width on the coupling efficiency for different polymer thicknesses, $w_{\text{polymer}} = 5\ \mu$m; (f) Taper coupling efficiency versus polymer width for different taper tips, $t_{\text{polymer}} = 1\ \mu$m.

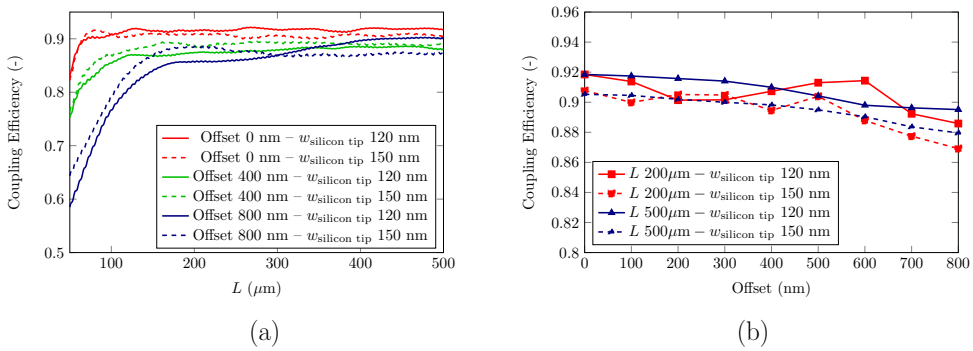

Figure 12. Overall coupling structure. (a) Coupling efficiency versus taper length for different lateral alignment offsets; (b) Coupling efficiency versus lateral alignment offset.

sensitivity for taper tip width.

Since the influence of the polymer thickness on the SOI taper coupling section is rather small for taper tips of 150 nm or smaller, the polymer thickness should be chosen to accommodate optimal III-V to polymer coupling. To allow the possibility of using the silicon to create for example a grating underneath the III-V waveguide to make distributed feedback lasers, an *n*-InP thickness of 200 nm is used for the remainder of the simulations [24]. This results in an optimal polymer thickness of 1 μm.

Figure 11(f) shows that the width of the polymer waveguide has hardly any influence on the coupling efficiency from polymer to silicon.

3.3. Overall coupling structure – lateral misalignment tolerance

Figure 12(a) shows the coupling efficiency versus taper length for different lateral alignment offsets (*y*-direction) of the silicon waveguide with respect to the III-V waveguide, both for silicon taper tip widths of 120 nm and 150 nm. A polymer thickness of 1 μm and a polymer width of 5 μm are assumed. The larger the lateral alignment offset, the longer the taper should be to reach a certain coupling efficiency. In Fig. 12(b) the coupling efficiency is shown as a function of lateral alignment offset for a fixed taper length of 200 μm and of 500 μm. At a length of 200 μm, fluctuations can be observed in the curve, meaning that the taper is not perfectly adiabatic yet. As expected, the fluctuations are larger for smaller taper tips for a fixed length, since the taper width changes more rapidly and the taper is thus less adiabatic. By increasing the length to 500 μm, adiabatic coupling is achieved. Since the taper is no part of the transfer printed structure, the length can be chosen freely. However, since the fluctuations are small, very long tapers are not necessary. As more than 90% of the light is coupled into the fundamental mode, only a small fraction of the light couples to higher order modes. Moreover, at the end of the coupling structure, light is coupled into a single mode waveguide, which means that the higher order modes will not be present in the remaining optical circuit. The coupling efficiency varies only a few percent with increasing lateral alignment offset, resulting in a very robust coupling performance. Figure 13 shows the overall optimised coupling structure. Mode profiles along the coupler show the adiabatic mode transformation from the III-V to the SOI waveguide. Finally Fig. 14 shows the wavelength dependence of the coupling structure, both at 0 nm and 800 nm lateral alignment offset. Simulations indicate that this structure will work efficiently in the complete C and L band.

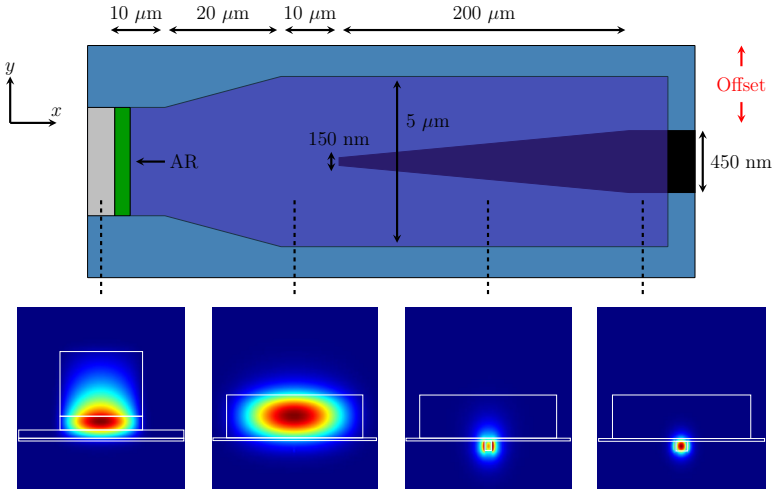

Figure 13. Overall coupling structure. Light propagation from the III-V waveguide to the SOI waveguide in the overall coupling structure. Mode profiles along the coupler are indicated as well.

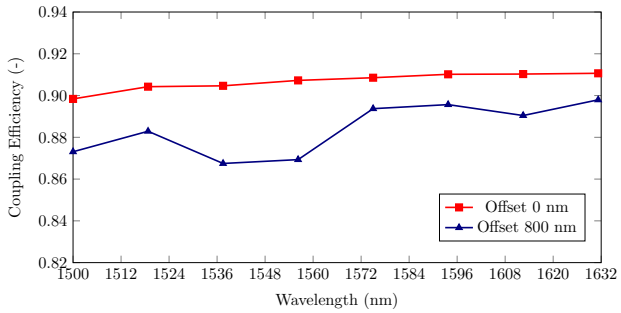

Figure 14. Wavelength dependence of the coupler efficiency for the overall optimised coupling structure with polymer intermediate waveguide.

4. Conclusion

In this paper two novel tapered couplers for adiabatic mode conversion in active III-V/SOI devices have been presented. The first coupler makes use of a broad and thick *n*-InP waveguide to which light is coupled as an intermediate step. This greatly enhances the misalignment tolerance, which is needed to comply with the current requirements for high-throughput transfer printing. The second coupler makes use of a polymer as intermediate waveguide such that less III-V processing is needed to fabricate the structure. Supported by optical simulations the coupling structures have been shown to exhibit efficient and very alignment tolerant coupling over a broad wavelength range covering the C and L band. The proposed couplers are expected to facilitate transfer-printing based heterogeneous integration of processed active III-V membrane devices on both passive and active SOI platforms.

Acknowledgments

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